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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,877	10/02/2003	Taiji Noda	60188-670	8100

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,877	NODA, TAIJI	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *15-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-02-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's election filed on March 10, 2005. Claims 1-17 are pending, in which claims 15-17 are non-elected without traverse as treated.

Election/Restrictions

1. Applicant's election filed of Group I, method claims 1-14 in Paper Mail dated March 10, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, and because the election is implicitly "without traverse", the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 15-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention.

Claim Rejections - 35 USC § 112

3. Claims 1-5 and 8-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

** In base claim 1, meaning and scope of "...heavy ions with relatively large mass..." are unclear and indefinite for how "heavy" and "large" of the ions.

** Re claim 8, last line, meaning and scope of "relatively shallow" are unclear and indefinite, since it is relative with respect to which region.

** Re base claim 10: the phrase "...of claim 1, further comprising, between the second and third steps..." is lacking proper antecedent basis, since there is no third step in claim 1. (Dependent claims are rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1,2,6-9,13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Noda et al (6,432,802).

Noda et al teach a method for forming a semiconductor device comprising at least the steps of: implanting, into a channel formation region of a semiconductor substrate 300, first dopant ions of a first conductivity type of indium ions, which are heavy ions with a relatively large mass number, to form a dopant implantation layer 303/306A in the channel formation region (Figs 5a-5c; col 12, lines 1-34, 18-25); and implanting a second dopant ions into the semiconductor substrate 300 to form an amorphous layer expanding from the substrate surface to a region of the substrate deeper than the dopant implantation layer 303 (Figs 5d; col 12, lines 35-55). Re claim 2 , wherein the semiconductor substrate 100 is made of silicon, and the second dopant ion of germanium belongs to group IV elements (col 12, lines 1-5; lines 35-50; col 13, lines 59-65). Re claim 6, wherein the heavy ions are indium ions (col 12, lines 18-25, lines 1-5). Re claim 7, wherein the dose of the heavy ions of indium to be implanted is 5x $10^{13}/cm^2$ or more (col 12, lines 18-25). Re claim 8, after the second step, a third step of performing a first thermal treatment to diffuse the first dopant ions from the dopant implantation layer (col 12, lines 5-13, lines 56-65), thereby forming a first diffused layer of the first conductivity type in the channel formation region, a fourth step of selectively forming a gate insulating film 310 on the semiconductor substrate and a gate electrode 302 on the gate insulating film 310 (Fig 5a-5d; col 12, lines 12-18), a fifth step of implanting third dopant ions of a second conductivity type into the semiconductor substrate using the gate electrode as a mask (Figs 5b-5d; col 12, lines 12-34), and a sixth step of performing a second thermal treatment on the semiconductor substrate to diffuse the third dopant ions, thereby forming a second diffused layer 305A of the second conductivity type whose junction position is relatively shallow (Figs 5b-5d; col 12, lines 56-65). Re claim 9, wherein the first heat treatment is RTA at a temperature of 950-1050°C at a rate of 100°C/sec and keep at about 10 seconds (col 12, lines 4-12; lines 54-62). Re claim 13, between fourth and six steps, implanting fourth dopant ions of the first conductivity type using the gate

electrode 302 as a mask, where the second heat treatment performed in the six steps diffuses the fourth dopant ions to form a third diffused layer 306 of the first conductivity type below the second diffused layer 305 (Figs 5B-5D,6A; col 12, lines 18-34; and lines 56-67). Re claim 14, after the six step, forming sidewalls 307 of an insulating film on the side surfaces of the gate electrode 302 (Fig 6B; col 13, lines 1-7), and implanting fifth dopant ions of the second conductivity type using the gate electrode 302 and the sidewalls 307 as a mask, then fourth heat treatment to diffuse fifth dopant layer, thereby forming, outside the second diffused layer 305, a fourth diffused layer 304 of the second conductivity type which has a deeper junction interface than the second diffused layer 305 (Figs 6b-6c; col 13, lines 8-18).

6. Claims 1,8,10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Maszara et al (6,184,112).

Maszara teaches (at Figs 2A-3B,1; col 2, line 28 through col 3) a method for forming a semiconductor device comprising at least the steps of: implanting, into a channel formation region of a semiconductor substrate, first dopant ions 104 of germanium a first conductivity type of ions, which are heavy ions with a relatively large mass number, to form a dopant implantation layer 202 in the channel formation region (Figs 2A,3A; col 2, lines 66 through col 3, line 67); and implanting a second dopant ions 204 into the semiconductor substrate to form an amorphous layer 102 expanding from the substrate surface to a region of the substrate deeper than the dopant implantation layer 202 (Figs 2A,2B,1; col 2, lines 29-65; col 3, lines 20-45). Re claim 8, after the second step, a third step of performing a first thermal treatment to diffuse the first dopant ions from the dopant implantation layer, thereby forming a first diffused layer 102 of the first conductivity type in the channel formation region, a fourth step of selectively forming a gate insulating film 410 on the semiconductor substrate and a gate electrode 412 on the gate insulating film 410 (Fig4, col 4, lines 6-40; col 3, lines 54-59, lines 25-67), a fifth step of implanting third dopant ions of a second conductivity type into the semiconductor substrate using the gate electrode 410 as a mask, and a sixth step of performing a second thermal treatment on the semiconductor substrate to diffuse the third dopant ions, thereby forming a second diffused layer 402/404 of the second conductivity type whose junction position is relatively shallow (Fig4, col 4, lines 6-40; col 3, lines 25-67). Re claims 10-11, wherein, between the

second and third steps, the step of performing a third thermal treatment at such a low temperature of about 600°C so that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions (col 3, lines 23-35).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Noda et al (6,432,802) or Maszara et al (6,184,112), taken with Lin et al (5,171,703).

Noda et al teach a method for forming a semiconductor device as applied to claims 1,2, 6-9,13-14 above. Maszara teaches a method for forming a semiconductor device as applied to claims 1,8,10,11 above.

Noda or Maszara does not mention the use of {100} plane semiconductor substrate.

However, Lin teaches (at col 3, line 67 through col 4, line 3; col 1, line 20 through col 3) forming the semiconductor device by using {100} plane semiconductor substrate to minimize dislocation defects.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Noda or Maszara by using the {100} plane semiconductor substrate as taught by Lin. This is at least because of the desirability to minimize dislocation defects.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Noda et al (6,432,802) or Maszara et al (6,184,112), taken with Sundaresan (6,190,179).

Noda et al teach a method for forming a semiconductor device as applied to claims 1,2,

6-9,13-14 above. Maszara teaches a method for forming a semiconductor device as applied to claims 1,8,10,11 above.

Noda or Maszara lacks growing an epitaxial silicon on the semiconductor substrate.

However, Sundaresan teaches (at Figs 1-4; col 2, lines 16-64; col 3, lines 8-25) the desirability of growing an epitaxial silicon 16 on a semiconductor substrate 10.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Noda or Maszara by growing an epitaxial silicon on the semiconductor substrate as taught by Sundaresan. This is because of the desirability to form a reliable semiconductor device having good operating characteristics with a minimal degradation form short channel effects.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Noda et al (6,432,802) or Maszara et al (6,184,112), taken with Sonoda (6,696,341).

Noda et al teach a method for forming a semiconductor device as applied to claims 1,2, 6-9,13-14 above. Maszara teaches a method for forming a semiconductor device as applied to claims 1,8,10,11 above.

Noda or Maszara lacks having a strained silicon layer having a crystal lattice of a larger lattice constant than a normal lattice constant on the semiconductor substrate.

However, Sonoda teaches forming a strained silicon layer 3 having a crystal lattice of a larger lattice constant than a normal lattice constant on the semiconductor substrate 2/1 (Fig 1, col 8, line 58 through col 9)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Noda or Maszara by forming a strained silicon layer having a crystal lattice of a larger lattice constant than a normal lattice constant on the semiconductor substrate as taught by Sonoda. This is because of the desirability to reduce breakdown field so as to improve ESD resistance and protection of the semiconductor device.

11. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al (6,432,802) taken with Wang et al (6,368,928).

Noda et al teach a method for forming a semiconductor device as applied to claims 1,2,

6-9,13-14 above.

Re claim 10 Noda lacks, between the second and third steps, performing a third thermal treatment at such a temperature of so that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions, wherein the temperature is 400 to 600°C (re claim 11) for a time of 1 to 20 hours (re claim 12).

However, Wang teaches (at col 4, lines 6-31) after implanting the dopant ions, performing a third thermal treatment at such a low temperature of 450-650°C for a time of up to 3 hours (180 minutes) so that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Noda by performing a third thermal treatment at such a low temperature of 450-650°C for a time of up to 3 hours, as taught by Wang. This is at least because of the desirability to recover crystal damage and limiting diffusion of the implanted dopant ions so that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-16

Michael Trinh
Primary Examiner